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Linearity measurement of digitizers used in sampling-based digital impedance bridges by the method of permuting capacitors

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Abstract

Experimental studies of commercial PXI digitizers in terms of their use in primary impedance metrology are presented in the paper. The scope of the work includes the presentation of the permutation method and presentation of new physical model of permuting capacitor device developed at Silesian University of Technology (SUT). The spread of the parameters of the capacitors used proves that the developed device can be used as a reference standard for measuring the voltage ratio. The developed permuting device was used by the authors to measure nonlinearity errors of digitizers on boards NI PXI-4462 which is commonly used in National Metrology Institutes for impedance measurement purposes. The obtained results showed the nonlinearity errors at the level 10^{-6} and proved possibility of comparing standards with modulus ratios of 5:1 with an uncertainty of $5 \cdot 10^{-6}$ without the need to correct digitizer nonlinearity. Moreover, the results allowed the authors to select a digitizer with the lowest nonlinearity errors that is used in digital sampling impedance bridge being currently developed at SUT.

1. INTRODUCTION

In recent years there has been a rapid development of digital bridges adapted for the comparison of four-terminal pair (4TP) impedance standards [1-6]. The National Metrological Institutes (NMIs) are developing comparison systems using both quantum [1, 2] and non-quantum [3-6] AC voltage sources. Metrological institutes of less developed countries focus their scientific research on bridges using non-quantum digital AC voltage sources to work as voltage ratio standards. Accuracies achieved with this type of systems are at the level of $10^{-5} \div 10^{-6}$. Non-quantum digital impedance bridges can be divided into two groups, depending on the method of determining the standard voltage ratio:

1) the so-called sourcing bridges, in which the voltage ratio is reproduced using readings from digital-to-analog (D/A) converters [3, 4];
2) the so-called sampling or digitizing bridges, in which the impedance ratio is determined based on the voltage ratio measured by analog-to-digital (A/D) converters [5, 6].

Sourcing-type impedance bridges are currently being developed at few National Metrological Institutes in Europe, e.g. at Istituto Nazionale Ricerca di Metrologica (INRiM, Italy) and National Standards Authority of Ireland (NSAI, Ireland). In contrast, sampling-type impedance bridges are being developed at Swiss (METAS), Danish (Trescal), Czech (CMI) and Polish (GUM) National Metrology Institutes. Sampling-type impedance bridge at Central Office of Measures in Warsaw is being currently developed in cooperation with scientists from the Silesian University of Technology. The work is carried out as part of the research project titled "Research and development of digital methods for four-port impedance comparison", which received funding under the "Polish Metrology" program. One of the important research topics undertaken in the project is to expand the range of compared impedances to enable comparisons of standards with ratios from 1:1 to 10:1. This will enable the transfer of the impedance units to multiples and submultiples of the fundamental at a relatively low cost and with accuracy at the level of single μΩ/Ω.

One of the basic errors in sampling-based bridge, affecting the results of impedance comparison having different modules is the error resulting from the nonlinearity of the digitizer used. The test results carried out for PXI digitizers typically used in impedance bridges proved that nonlinearity errors cannot be ignored in the analysis and may determine the accuracy of the impedance measurement bridge [7].

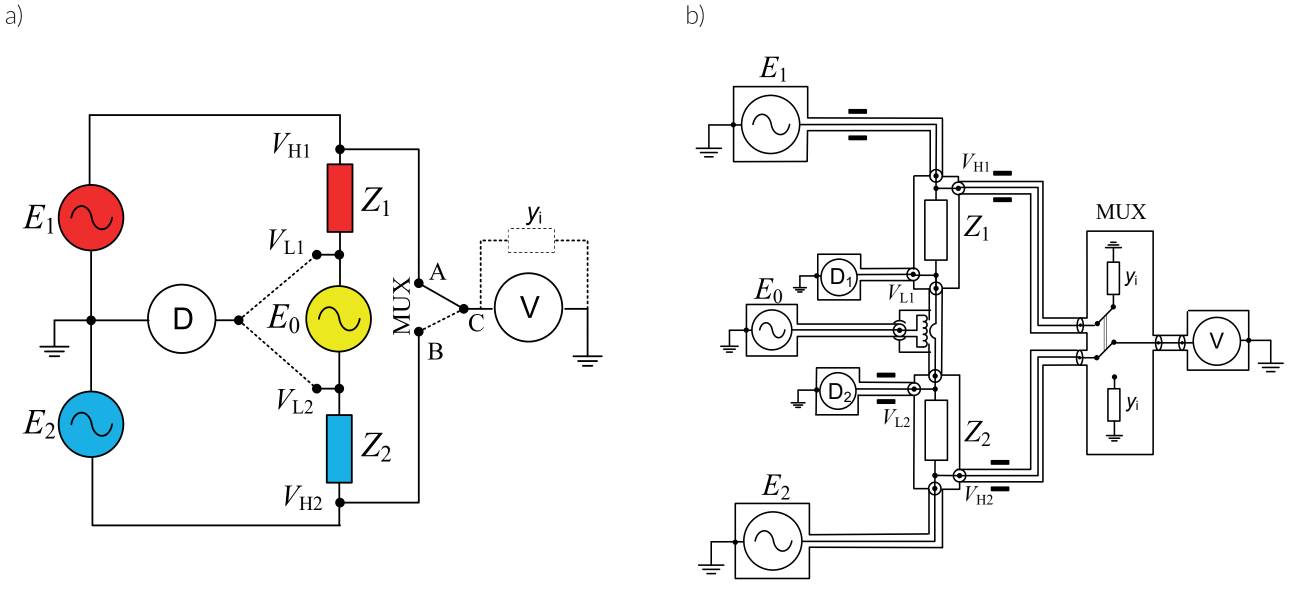
Therefore, in sampling bridges based on measurement of the complex voltage ratio using a digitizer, it is necessary to measure and possibly correct nonlinearity errors of the digitizer (or sampler). This measurement is not an easy task because it requires reproducing the reference voltage ratio with extremely high accuracy (at least 10^{-7}). In practice, it leads to the fact that metrological institutes use the so-called permutation or build-up method (see Section 3). Since systems using the above-mentioned methods are not commercially available, scientists working at NMIs are forced to design and test such systems.

The paper is organized as follows: in Section 2 and 3 the structure of the sampling-based bridge developed at SUT and GUM and the problem of the bridge linearity are described. In Section 4.1 and 4.2 theory of permutation and physical model of permuting capacitors developed at SUT are presented. System designed for nonlinearity measurements and nonlinearity results obtained for PXI-4462 digitizers are given in Section 4.3. Finally, the conclusions of this work are presented in Section 5.

2. SAMPLING-BASED BRIDGE

The sampling-based digital impedance bridge shown in Fig. 1 is based on coherent sequential sampling of voltages V_{H1} and V_{H2} across the compared impedances Z_1 and Z_2. The system is balanced by changing the amplitude and phase of one of the main sources (E1 or E2) and the auxiliary source E_0. In the equilibrium state of the bridge (V_{L1}=V_{L2}=0) the impedance ratio is determined based on samples obtained using the digitizer "V" switched between the compared objects using the multiplexer MUX. The following relationship is used:

$$\Gamma = \frac{\boldsymbol{Z_1}}{\boldsymbol{Z_2}} = -\frac{\boldsymbol{V_{H1}}}{\boldsymbol{V_{H2}}} \tag{1}$$



🟥 Fig. 1. 4TP sampling-based impedance bridge: a) schematic diagram, b) coaxial implementation

Since the voltages across the compared impedances are measured using the same digitizer, swapping of the standards is not necessary in this case. However, it is still advisable to use this procedure when buffers with high input impedance are used at the multiplexer inputs (potentials V_{H1} and V_{H2}).

The coaxial implementation of the sampling bridge is shown in Fig. 1b. The use of a coaxial four-terminal pair circuit (4TP) guarantees immunity to external electromagnetic interferences. Moreover, the unwanted electromagnetic radiation of such system is strongly reduced [8]. In the actual system, a precise two-phase AC voltage source designed and built at the Silesian University of Technology (SUT) was used as the main sources E_1 and E_2. Details regarding the construction and test results of the source used are presented in [9]. The structure of the bridge and the results of system validation are presented in [10-12]. 4TP resistance and capacitance standards designed and built by scientists from the SUT and employees of the GUM were used for validation. Details on the construction of impedance standards and results of their stability are presented in [13]. The results of research carried out at SUT, the GUM and the Swiss National Metrology Institute (METAS) confirmed the accuracy of the system reaching 10^{-6} when comparing standards with impedances ranging from several hundred Ω to several dozen kΩ carried out at frequencies from 100 Hz to 5 kHz [10].

3. DIGITIZER'S NONLINEARITY

When measuring the ratio of two quantities (like in the ratio comparator bridge), we are much more interested in linearity than the accuracy of the instrument. This is due to the fact that it is the non-linearity error that determines the measurement accuracy in this case, other errors are reduced by determining the ratio. It is therefore common approach that manufacturers of precision measurement instruments include information about linearity (sometimes called "transfer accuracy") in addition to accuracy.

The result of the ratio impedance comparison using the sampling-based comparator bridge expressed in equation (1) is sensitive to the nonlinearity errors of the digitizer V. Due to the digitizer errors in the real measurement system, the voltage V_{H1} and V_{H2} differ from the read values, as presented in Fig. 2.

If the digitizer gain is the same for different voltages (in other words, the digitizer is linear as in Fig. 2a), then the gains cancelled when measuring voltage ratio. However, if the digitizer gain is different for different voltages (nonlinear sampler, see Fig. 2b), then errors occur in the measurement of the complex voltage ratio. It can be shown that for the sampling bridge without applying swapping procedure, the relative voltage ratio error $\frac{\Delta\Gamma}{\Gamma}$ resulting from the digitizer's nonlinearity is expressed by the equation [14]:

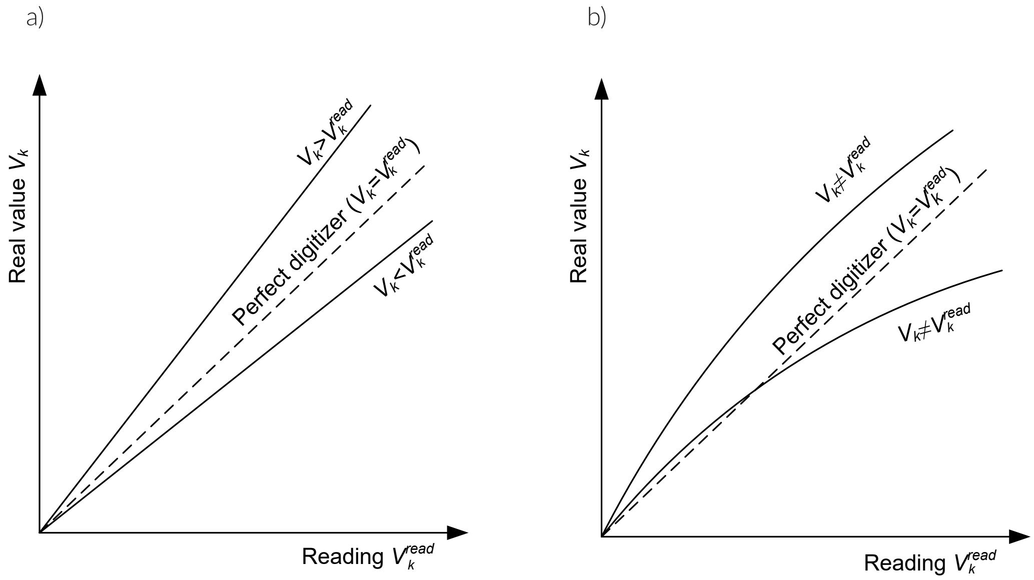


Fig. 2. Characteristics of digitizers: a) linear digitizer; b) nonlinear digitizer

$$\Gamma = \frac{\boldsymbol{Z_1}}{\boldsymbol{Z_2}} = -\frac{\boldsymbol{V}_{\mathbf{H1}}}{\boldsymbol{V}_{\mathbf{H2}}} \tag{2}$$

where: g – gain of the digitizer, a V_i^{read} – voltage value measured by the digitizer.

The gains appearing in equation (2) can be determined:

1) using a standard voltage ratio (e.g. reproduced by an inductive voltage divider IVD [15]) or a standard impedance ratio;
2) using the permuting capacitors method [16] or the build-up method [17].

The method with a standard impedance ratio was used by the authors of the work when testing the precise six-channel AC voltage source, developed at the University of Zielona Góra (UZG) and used to power a sourcing bridge developed and implemented in the Italian National Metrology Institute (INRiM). The research was carried out during a research internship of one of the authors of the work at the INRiM in 2018, using capacitance standards with values of 1 nF, 2 nF and 5 nF. The standard capacitance ratios of 1:1, 1:2 and 1:5 were determined on the basis of capacitance measurements with a precise Andeen-Hagerling AH2700 bridge with a nonlinearity error of $1{\cdot}10^{-6}$. The results of measurements performed at 1 kHz and 1.6 kHz are presented in [16]. The obtained results indicate the need to correct nonlinearity errors in case the comparator bridge will be used to compare impedances with significantly different modules (ratios above 2:1) with an uncertainty of 10^{-6}.

The nonlinearity errors of digitizers used in the sampling bridge currently being developed at KMEiA and GUM were initially determined using a method using the standard 7-decade ESI Dekatran DT72A inductive voltage divider. Detailed test results obtained for voltage ratios from 0.2 to 1 can be found in [18]. Since, according to the manufacturer's specification, the voltage ratio setting errors for the voltage divider used exceed 2 µV/V, the tests performed using this method are for information purposes only and cannot be used to correct the digitizer errors. It was therefore necessary to develop a system that would ensure the possibility of determining nonlinearity errors with an uncertainty of at least 10^{-7}. A device using permuting capacitor method was proposed.

4. CAPACITORS' PERMUTATION METHOD

4.1. Theoretical basics

The capacitor permutation method, known for many years [16], is based on a system of capacitors with possibly equal capacitance that can be connected in parallel. In recent years, due to the development of technology allowing the construction of capacitors (especially those with NP0 dielectric) with very low temperature coefficients, there has been an increase in interest in this method, especially among researchers from NMIs [19].

To realize standard n:1 ratio, where n=1…10, n+1 capacitors are needed. For example, eleven capacitors are needed to realize standard 10:1 ratio. In the case of a bridge system, one of the capacitors is placed in the upper branch of the bridge (Z_1 in Fig. 1), and the others in its lower branch (thus creating impedance Z_2). Then, the capacitor in the upper branch is cyclically rearranged (permuted) and replaced with one of the capacitors previously connected in parallel in the lower branch of the bridge. The permutation sequence is repeated (n+1) times until each capacitor is in the upper branch of the bridge. The theoretical basis of the method is the averaging of errors (understood as the deviation of the capacitance from the average value) of the voltage ratio for all (n+1) permutations. The realization of the standard voltage ratio is the better, the smaller are the deviations in the capacitance of each capacitor during the entire measurement cycle.

Let us analyze the case of the standard impedance ratio of 2:1. To realize such a ratio, three capacitors with possibly equal values are needed. Capacitance equalization is extremely important here, as discussed later in the paper. The capacitors are placed in the two arms of the bridge, as shown in Fig. 3.

According to formula (1), the voltage ratios for permutations No. 1, 2 and 3, respectively, can be determined from the following equations:

$$\Gamma_1 = \frac{Z_1}{Z_2} = \frac{C_2 + C_3}{C_1} \tag{3}$$

$$\Gamma_2 = \frac{C_1 + C_3}{C_2} \tag{4}$$

$$\Gamma_3 = \frac{C_1 + C_2}{C_3} \tag{5}$$

Since the nominal values of the capacitors are the same, denoting the capacitor errors by $\delta_1, \delta_2, \delta_3$ respectively, we have

$$\Gamma_1 = \frac{C_2 + C_3}{C_1} = \frac{C(1+\delta_2) + C(1+\delta_3)}{C(1+\delta_1)} \tag{6}$$

$$\Gamma_2 = \frac{C_1 + C_3}{C_2} = \frac{C(1+\delta_1) + C(1+\delta_3)}{C(1+\delta_2)} \tag{7}$$

$$\Gamma_3 = \frac{C_1 + C_2}{C_3} = \frac{C(1+\delta_1) + C(1+\delta_2)}{C(1+\delta_3)} \tag{8}$$

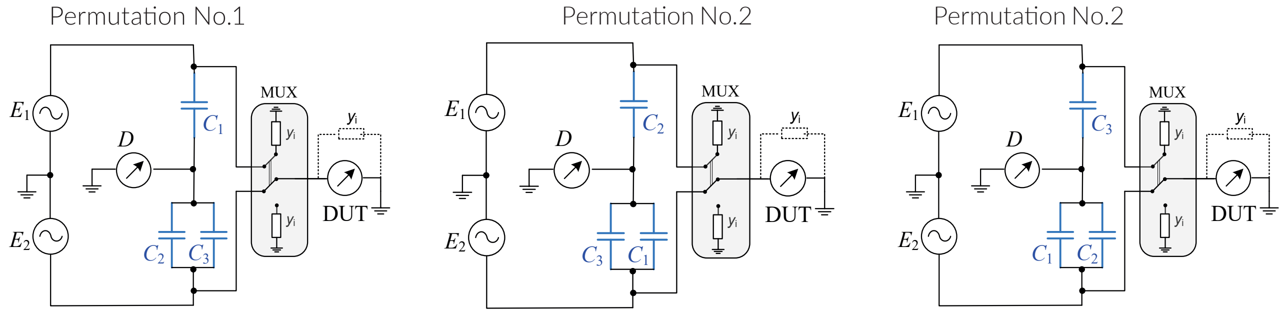


Fig. 3. Capacitors permutation to realize standard voltage ratio 2:1

After averaging the above ratios, we get:

$$\Gamma = \frac{\Gamma_1 + \Gamma_2 + \Gamma_3}{3} = \frac{C^3(1+\delta_2)^2(1+\delta_3) + C^3(1+\delta_3)^2(1+\delta_2) + C^3(1+\delta_1)^2(1+\delta_3)}{3C^3(1+\delta_1)(1+\delta_2)(1+\delta_3)} + \frac{C^3(1+\delta_3)^2(1+\delta_1) + C^3(1+\delta_2)^2(1+\delta_1) + C^3(1+\delta_1)^2(1+\delta_2)}{3C^3(1+\delta_1)(1+\delta_2)(1+\delta_3)}, \tag{9}$$

which, after simplifying and omitting the second- and third-order components, gives:

$$\Gamma = \frac{6C^3(1+\delta_1+\delta_2+\delta_3)}{3C^3(1+\delta_1+\delta_2+\delta_3)} = 2 \tag{10}$$

As mentioned, the above analysis omitted the second- and third-order components. This is only possible if the relative errors of individual capacitors are no greater than 10^{-4} (i.e. 0.01%). In this case, neglecting the second-order components will not result in a voltage ratio error greater than 10^{-8}.

A similar analysis to that carried out for the voltage ratio of 2:1 can be performed for the remaining voltage ratios (from 3:1 to 10:1), which corresponds to the use of 4 to 11 capacitors, respectively.

4.2. Physical model

As part of the research work carried out at KMEiA in the framework of the project which received funding under the "Polish Metrology" program, a precise device for testing the nonlinearity of digitizers was developed and manufactured, using the permuting capacitors method. This device, characterized by a fully symmetrical design, is made of a solid aluminum block with appropriate cells in which capacitors are placed. The stages of capacitor construction are shown in Fig. 4. They show, from the upper left to the bottom right: 1) an aluminium block with cells, 2) a cover with capacitors and connectors, 3) a block with polystyrene insulation with visible MUSA Metrology Grade coaxial connectors and

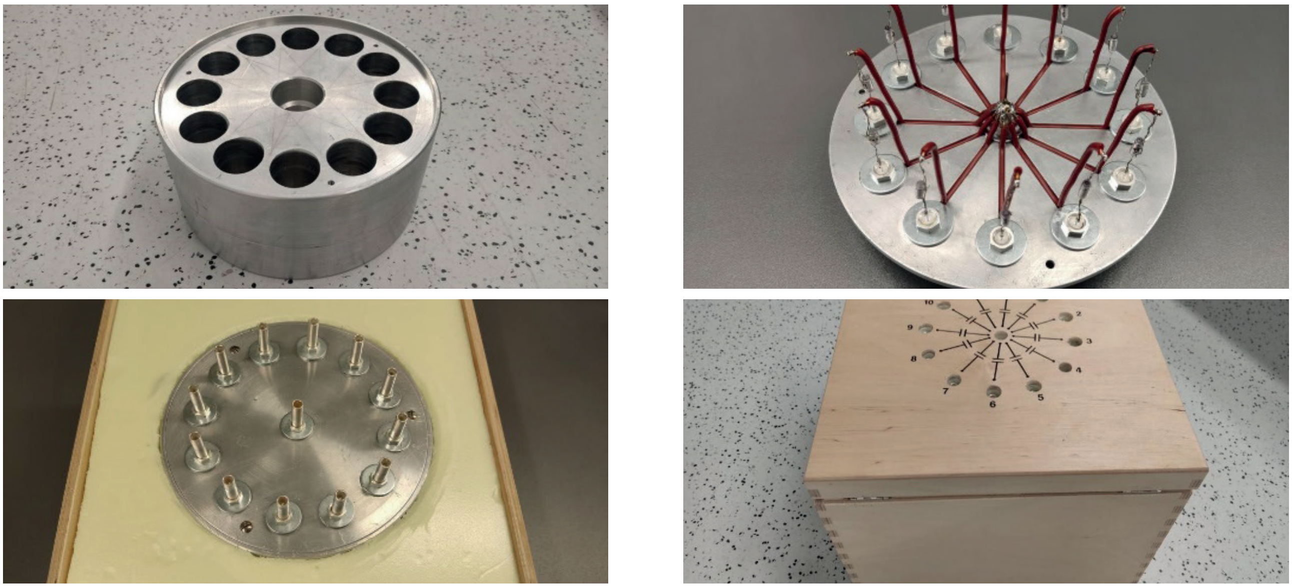


Fig. 4. Permuting capacitor device UP1

4) a view of the complete device. Styroflex capacitors with nominal values of 1.5 nF and SMD capacitors with NP0 dielectric, characterized by a relatively low temperature coefficient (nominally 0±30 ppm/°C), were used for construction of the permuting capacitor device.

In order to equalize the capacitance of all eleven nominally equal capacitors, capacitance measurements were made using a precise Agilent E4980A impedance bridge. After equalizing the capacitance using SMD capacitors with values from 1 pF to 4 pF, final measurements were made within a few days at two different ambient temperatures. The measurement results are presented in Table 1.

Table 1. The results of capacitance measurements

Designation	C , nF at 22.5°C	C , nF at 24.5°C
C_1	1.50213	1.50182
C_2	1.50217	1.50179
C_3	1.50203	1.50171
C_4	1.50193	1.50155
C_5	1.50201	1.50162
C_6	1.50199	1.50161
C_7	1.50194	1.50157
C_8	1.50198	1.50156
C_9	1.50198	1.50157
C_{10}	1.50222	1.50183
C_{11}	1.50206	1.50167
AVG [nF]	1.50204	1.50166
Std. deviation [nF]	0.00009	0.00010
Max. relative error [-]	0.0001	0.0001

The maximum relative deviation of the capacitor value from the average is 10^{-4}, therefore the series meets the accuracy requirement referred to in Section 4.2.

In order to enable parallel connection of any number of capacitors (from 2 to 11 pieces), an appropriate chain of cables equipped with MUSA connectors was made (it is visible in the bottom left corner in Fig. 5)

4.3. Results

Nonlinearity measurements of four digitizers (denoted as AI0, AI1, AI2, AI3) boarded at the PXI-4462 data acquisition module with serial number E1A5A2 were carried out at the Laboratory of Precise Electrical Measurements of the SUT. Before starting the tests, in accordance with the manufacturer's recommendations, the auto-calibration procedure of the PXI module was performed [12]. Both the sampling system and the source were properly heated. The tests were carried out in an electromagnetically shielded and thermally stabilized room. The temperature was (23.0±0.5)°C. The measurements were performed in the circuit shown in Fig. 1 where Z_1 and Z_2 were made up from a certain number of capacitors (as presented in Fig. 3 in the case of three capacitors). The appearance of the measurement setup is shown in Fig. 5. The tests were carried out at a frequency of 1 kHz, at which impedance standard comparisons are most often performed. The voltage ratios were determined based on samples collected from five series of switchings. Each of these series, consist of ten complete data sets (as shown in the "Aquired Data" window in Fig. 6). One set contained at least 64 sinewave periods.

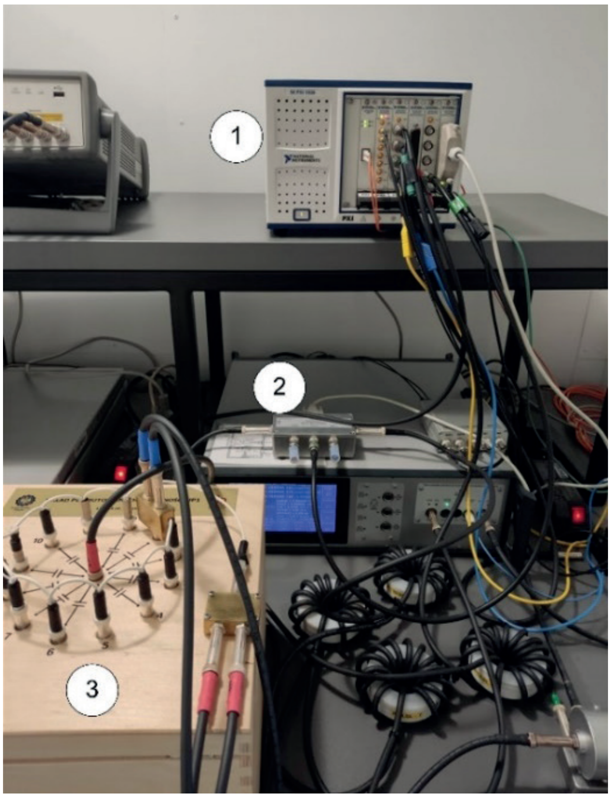
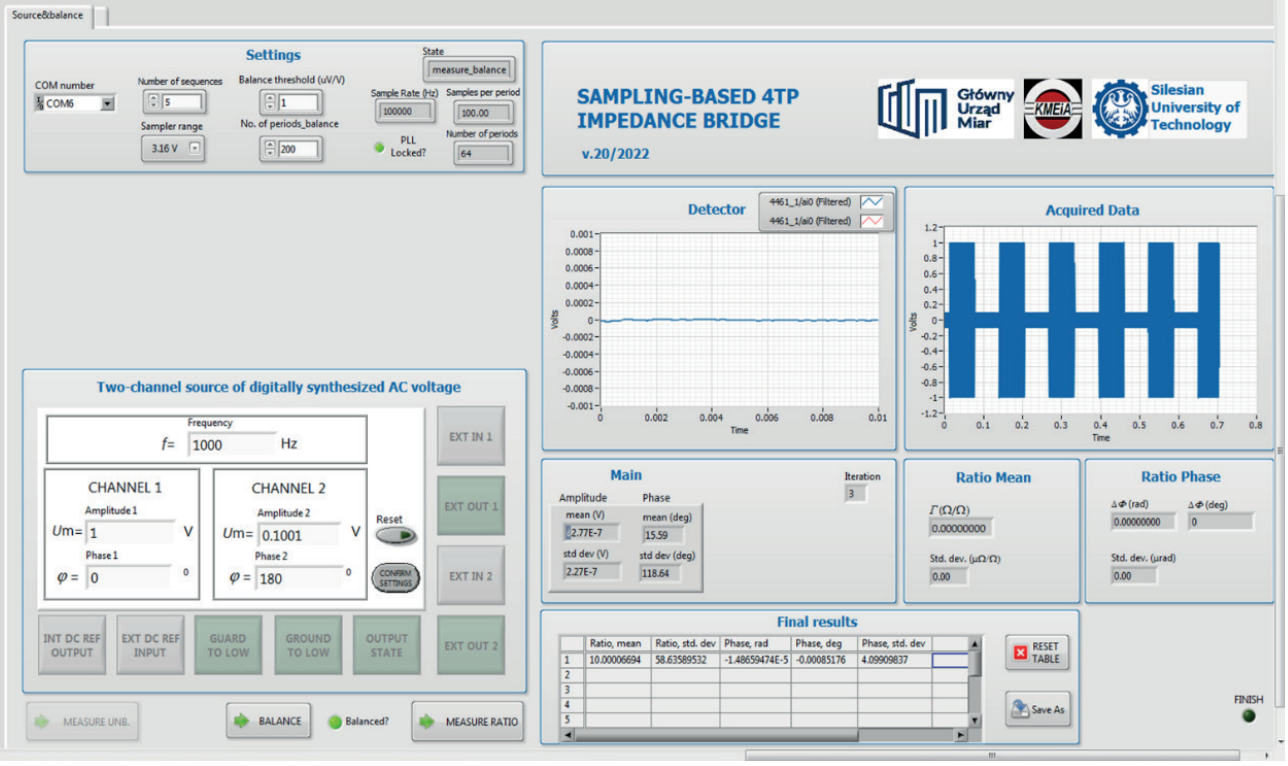


Fig. 5. Photograph of the setup for linearity investigation: 1 – PXI sampling system, 2 – precise two-phase AC voltage source built at SUT, 3 – permuting capacitor device designed at SUT

The control software (Virtual Instrument, VI) was prepared to measure the voltage ratio on the switched capacitors. The program responsible for the bridge balancing process and data acquisition was written in the LabVIEW environment. The secant method described in [20] was used to balance the bridge. Main window of the program is shown in Fig. 6.

The DFT algorithm was used to determine the RMS values of AC voltages. The sampling frequency was 100 kHz. The measurement results of the relative nonlinearity errors of the digitizers are presented in Fig. 7. The ratio



State: measure_balance

COM number: COM6

Number of sequences: 5

Sampler range: 3.16 V

Balance threshold (uV/V): 1

No. of periods_balance: 200

Sample Rate (Hz): 100000

Samples per period: 100.00

PLL Locked?

Number of periods: 64

Frequency $f=$ 1000 Hz

Amplitude 1 $Um=$ 1 V

Phase 1 $\varphi=$ 0 °

Amplitude 2 $Um=$ 0.1001 V

Phase 2 $\varphi=$ 180 °

Iteration: 3

Amplitude mean (V): 2.77E-7

Amplitude std dev (V): 2.27E-7

Phase mean (deg): 15.59

Phase std dev (deg): 118.64

Γ(Ω/Ω): 0.00000000

Std. dev. (μΩ/Ω): 0.00

ΔΦ (rad): 0.00000000

ΔΦ (deg): 0

Std. dev. (μrad): 0.00

	Ratio, mean	Ratio, std. dev	Phase, rad	Phase, deg	Phase, std. dev	
1	10.00006694	58.63589532	-1.48659474E-5	-0.00085176	4.09909837	
2						
3						
4						
5						

Fig. 6. A screenshot of the LabVIEW VI developed to measure nonlinearity errors

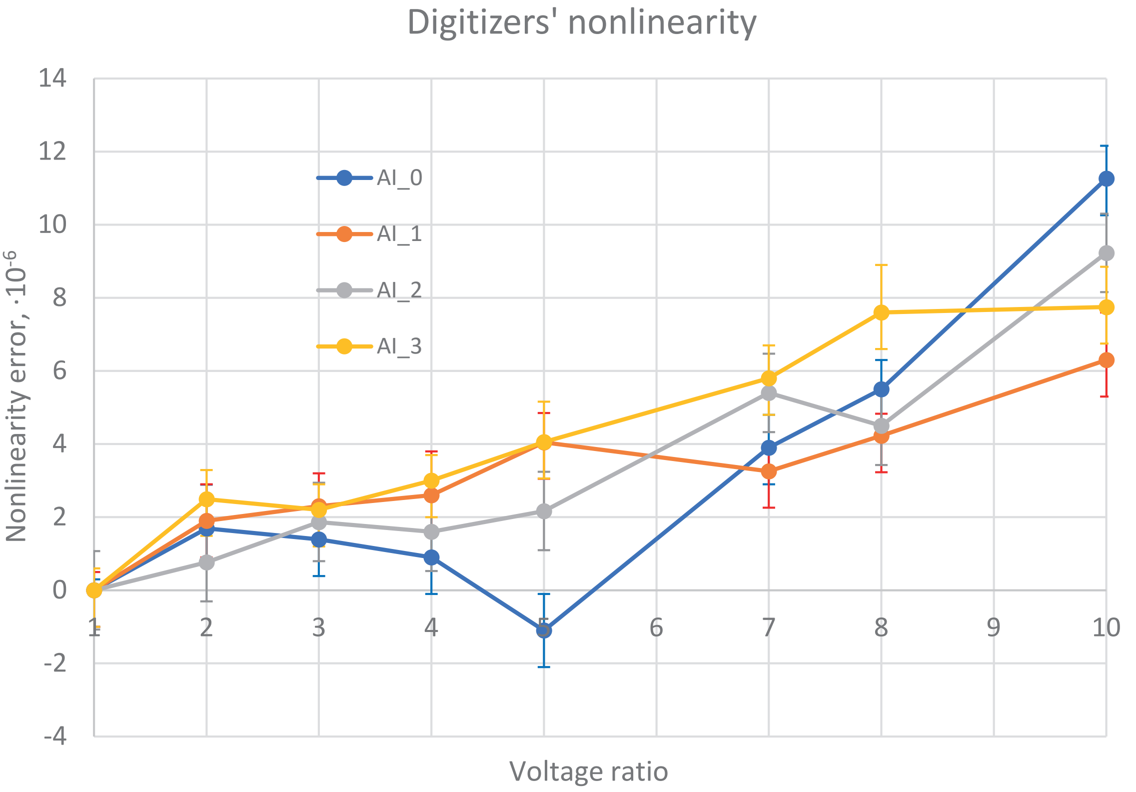


Fig. 7. Nonlinearity results of PXI digitizers: error bars correspond to type A uncertainty.

of the voltages on the abscissa corresponds to the ratio of the compared impedances. Error bars correspond to type A uncertainties of voltage ratio measurements. They did not exceed 1.2 µV/V. As expected, the nonlinearity errors increase as the ratio of the measured impedances increases. The obtained results prove that for the comparison of impedance standards with a modulus ratio ranging from 1 to 5, nonlinearity errors do not exceed 4 ppm. Therefore, assuming the comparison uncertainty at the level of $5{\cdot}10^{-6}$, there is no need to correct the nonlinearity errors in the system. For the ratio modulus equals 10, the nonlinearity errors range from 6 to 11.5 ppm. Therefore, in order to ensure the comparison uncertainty at the level of $5{\cdot}10^{-6}$, software correction of digitizer nonlinearity errors is necessary. Since the errors are systematic in nature, they can be corrected in the form of corrections during the calculation of the complex voltage ratio.

The AI_1 digitizer has the best metrological properties, so this digitizer is currently used in the sampling bridge developed at the Silesian University of Technology.

In order to investigate the possible impact of sampling frequency on the results of digitizers' nonlinearity, the tests were repeated for a frequency of 1592 Hz. This frequency is also often used in impedance comparisons. The nonlinear errors in this case did not differ from those obtained for the frequency of 1 kHz by more than 1 µV/V.

4.4. Summary

This work presents the results of nonlinearity error measurements of PXI-4462 digitizers used at the KMEiA in Gliwice and at the GUM in Warsaw to build sampling-based impedance bridges. The main novelty of the paper is to show the possibility of high-precision measurements (at the accuracy level 10^{-7}) of digitizer nonlinearity errors using a permutation method. For this purpose, an innovative permuting capacitor device was built at SUT using specially selected and tested capacitors. The obtained results showed that the nonlinearity errors of PXI digitizers do not exceed 12 ppm in the ratio range up to 10:1. Moreover, the obtained results proved the possibility of comparing standards with modulus ratios of 5:1 with an uncertainty of $5{\cdot}10^{-6}$ without the need to correct digitizer nonlinearity errors. Moreover, the test results allowed us to select a digitizer with the lowest nonlinearity errors in order to use it to measure the complex voltage ratio in the sampling impedance bridge.

It is worth emphasizing that the permuting capacitors device designed and manufactured at the SUT require manual switching between individual configurations, which significantly extends the measurement time. This may cause an uncontrolled change in capacitance resulting from slightly different temperature coefficients of the capacitors. Although the UP1 device is well thermally insulated with a thick (5-10 cm) layer of extruded polystyrene (XPS), it is not fully temperature stabilized. In the case of such a device, a change in the ambient temperature negatively affects the accuracy of the determined voltage ratio. Moreover, it is impossible to fully automate the measurements.

The solution to both problems is to build an automatic system of permuted capacitors, where switching is carried out using relays. Therefore, an attempt was made to build such an electronic switching system, being aware of many problems that need to be solved during design (such as: isolating interference-generating elements, eliminating inductive couplings, very good magnetic and electrical shielding, equalizing parasitic capacitances, thermal stabilization of capacitors). Currently, this system is undergoing detailed tests and in case of positive test results it will replace the UP1 manual device in the near future.

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